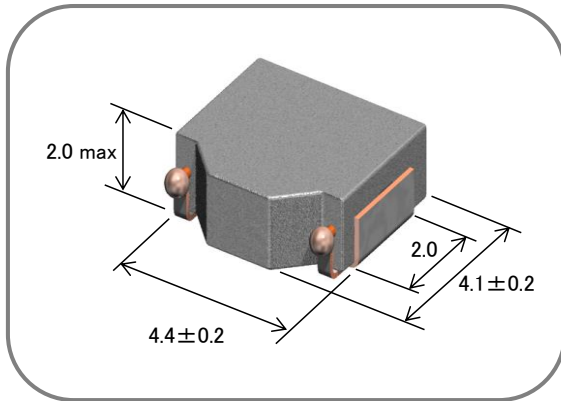


Component Image & Dimension



Features

Sampling Stage

- a) Small Footprint and Low Profile Design :
Footprint : 4.4 x 4.1 mm Typ.
Height : 2.0mm Max.
- b) High Power Handling Capability :
Small Copper Loss
Using Large Saturation Induction of Fe- based metals
- c) Flat inductance performance over temperature based on the high curie temperature of the iron powder core material.
- d) Automatic Mounting in Tape&Reel Package.

Applications

Note Book & Mobile Computer, VRM, Cellular Phone, HDD etc.

Electrical Specification

TDK Identification	Inductance		Test Freq. (kHz)	DC Resistance		Rated DC Current			
	at 0A (uH)	Tol. (%)		Spec. (m-Ohm)	Typ. (m-Ohm)	Idc 1 (A)		Idc 2 (A)	
※ SPM4020T- R22M-LR	0.22	+/-20%	100	6.5 max	5.9	11.5	15.3	9.2	9.7
SPM4020T- R27M-LR	0.27	+/-20%	100	9.7 max	8.8	11.0	14.6	7.9	8.3
SPM4020T- R33M-LR	0.33	+/-20%	100	9.7 max	8.8	10.9	14.5	7.9	8.3
SPM4020T- R47M-LR	0.47	+/-20%	100	11.8 max	10.7	10.6	14.1	7.2	7.5
SPM4020T- R68M-LR	0.68	+/-20%	100	17.9 max	16.3	7.4	9.8	6.7	7.0
※ SPM4020T- R86M-LR	0.86	+/-20%	100	21.3 max	19.4	7.1	9.5	5.5	5.8
SPM4020T- 1R0M-LR	1.00	+/-20%	100	28.1 max	25.5	6.9	9.0	5.3	5.6
SPM4020T- 1R5M-LR	1.50	+/-20%	100	39.9 max	36.3	4.7	6.3	4.5	4.7
SPM4020T- 2R2M-LR	2.20	+/-20%	100	61.6 max	56.0	4.0	5.3	4.2	4.4
SPM4020T- 3R3M-LR	3.30	+/-20%	100	74.3 max	67.5	3.8	5.0	3.3	3.5
SPM4020T- 4R7M-LR	4.70	+/-20%	100	140.8 max	128.0	2.6	3.5	2.4	2.5
※ SPM4020T- 5R6M-LR	5.60	+/-20%	100	146.8 max	133.5	2.4	3.2	2.0	2.1
※ SPM4020T- 6R8M-LR	6.80	+/-20%	100	178.7 max	162.5	2.3	3.0	1.9	2.0
※ SPM4020T- 8R2M-LR	8.20	+/-20%	100	203.3 max	184.9	2.0	2.6	1.8	1.9
※ SPM4020T- 100M-LR	10.00	+/-20%	100	263.0 max	239.1	1.9	2.5	1.6	1.7

Note. Idc 1 : Based on the inductance change.(-30% Reduction from Nominal L Value)

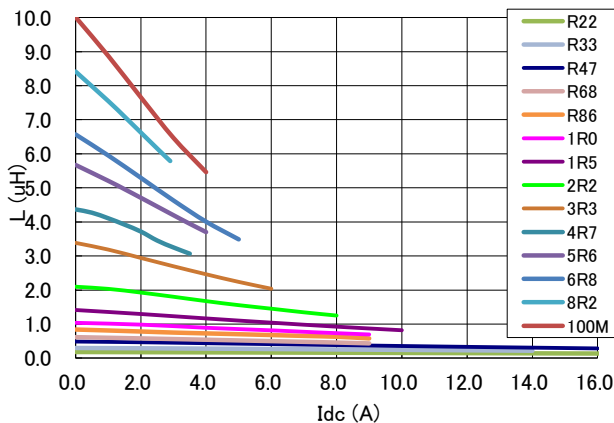
Idc 2 : Based on the self temperature rise. (+40 deg typ.)

Operating Temperature Range: -40 °C ~ +125 °C (including self temperature rise)

Caution: Please contact our sales person when you consider organic solvent or aqueous cleaning.

※ Simulation Data

Inductance vs. DC Superposition



Recommended pad layout

